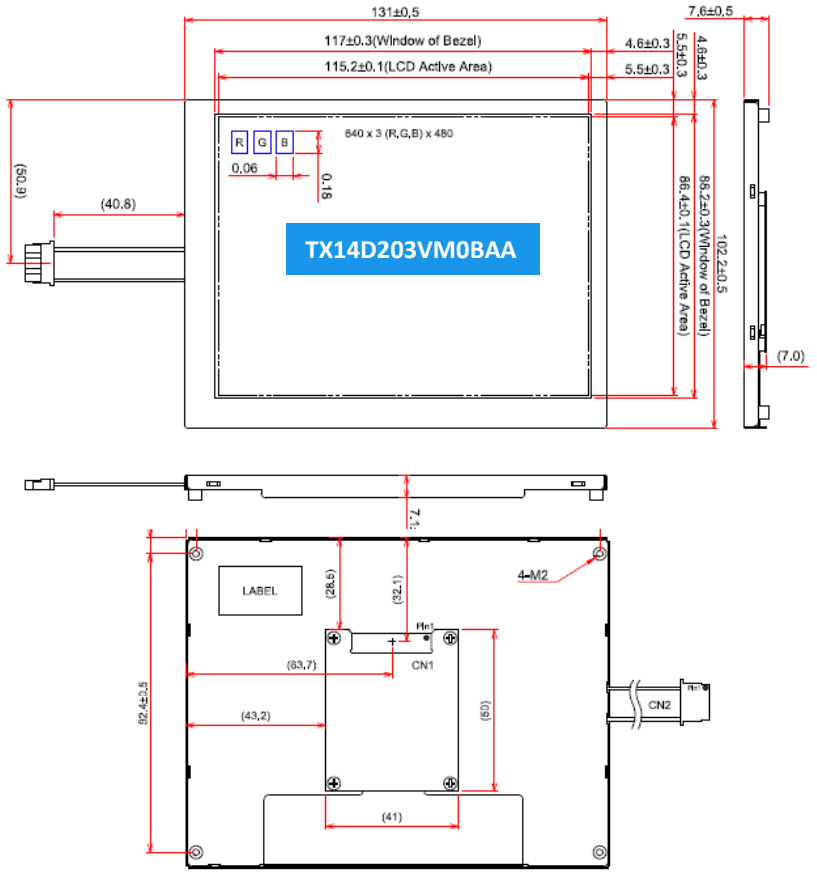
Japan Display Inc.

5.7” VGA
Specification comparison (PCN-1095)

28th Nov. 2023

SPEC comparison – CMOS interface

P/N	TX14D203VM0BAA/BPA	
Revision	A	B
Display Mode	a-Si TFT, Transmissive, Normally Black	←
Outline Dimensions(mm)	131.0(W) x 102.2(H) x 7.6(D)	←
Active Display Area (mm)	115.2(W) x 86.4(H)	←
Resolution	640(W) x 3(RGB) x 480(H)	←
Pixel Pitch(mm)	0.18(W) x 0.18(H)	←
Number Of Colors	262K Colors (6-bit RGB)	←
Interface	CN1: CMOS_40 pins (FA5S040HP1R3000) CN2: 3 pins (BHR-03VS-1)	←
NTSC	60%	←
Brightness(nits)	1000/800	←
Contrast Ratio	1000 : 1	←
Viewing Angle (U/D/L/R, CR>10)	85/85/85/85	←
Weight (g)	104/145	←
Top./Tst. (^{O}C)	-30~80 / -30~80	←
Input voltage (V)	LCD: 3.3 / Backlight: 12	←
LED lifetime (hrs)	50K	←
Timing	H/V + DE mode	←
Touch panel	4W R-T/P (option)	←



Note

In addition to the comparison table,

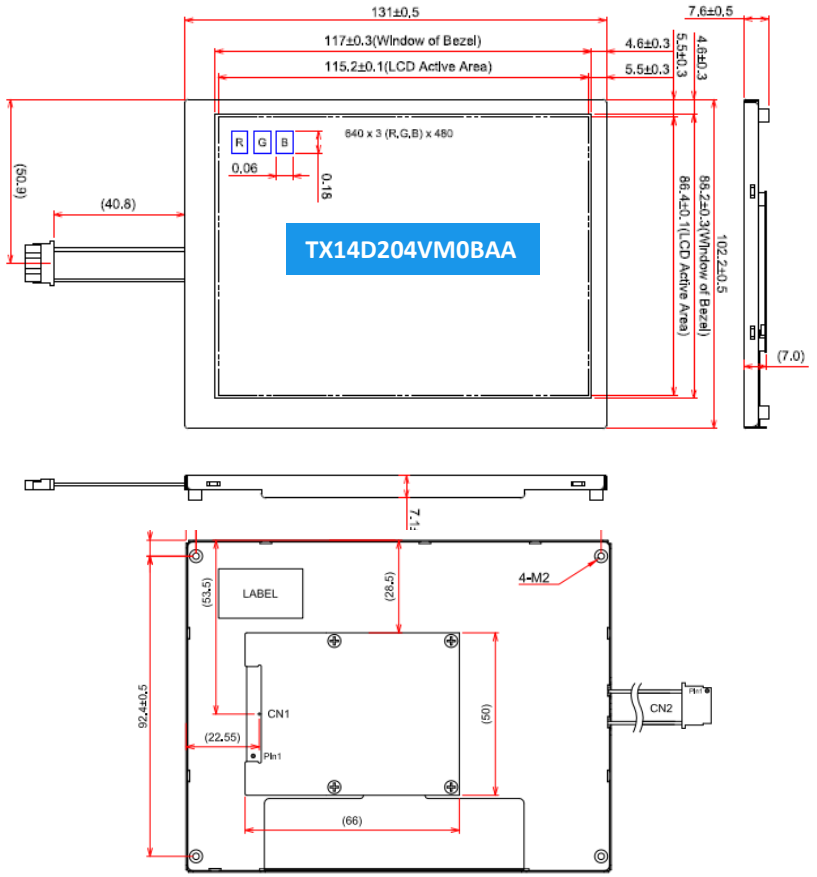
① Mechanical wise, Rev. A and Rev. B are identical.

② Electrical wise, Rev. A and Rev. B are identical.

③ Timing for driving the display, Rev. A and Rev. B are identical.

SPEC comparison – LVDS interface

P/N	TX14D204VM0BAA/BPA	
Revision	A	B
Display Mode	a-Si TFT, Transmissive, Normally Black	←
Outline Dimensions(mm)	131.0(W) x 102.2(H) x 7.6(D)	←
Active Display Area (mm)	115.2(W) x 86.4(H)	←
Resolution	640(W) x 3(RGB) x 480(H)	←
Pixel Pitch(mm)	0.18(W) x 0.18(H)	←
Number Of Colors	262K Colors (6-bit RGB)	←
Interface	CN1: LVDS_20 pins (FI-SEB20P-HF13E) CN2: 3 pins (BHR-03VS-1)	←
NTSC	60%	←
Brightness(nits)	1000/800	←
Contrast Ratio	1000 : 1	←
Viewing Angle (U/D/L/R, CR>10)	85/85/85/85	←
Weight (g)	108/149	←
Top./Tst. (^{O}C)	-30~80 / -30~80	←
Input voltage (V)	LCD: 3.3 / Backlight: 12	←
LED lifetime (hrs)	50K	←
Timing	H/V + DE mode	←
Touch panel	4W R-T/P (option)	←



Note

In addition to the comparison table,

① Mechanical wise, Rev. A and Rev. B are identical.

② Electrical wise, Rev. A and Rev. B are identical.

③ Timing for driving the display, Rev. A and Rev. B are identical..

SPEC comparison – Pin assignment

CMOS_Rev. A and Rev. B are identical

9.1 INTERFACE PIN CONNECTIONS

The display interface connector is FA5B040HP1R3000 made by JAE (Thickness: 0.3 ± 0.05mm; Pitch: 0.5 ± 0.05mm) and more details of the connector are shown in the section of outline dimension.

Pin assignment of LCD interface is as below:

Pin No.	Signal	Function	Pin No.	Signal	Function
1	V_{DD}	Power Supply for Logic	21	G4	Green Data
2	V_{DD}		22	G3	Green Data
3	UD	Vertical Display mode Control	23	V_{SS}	GND
4	LR	Horizontal Display mode Control	24	G2	Green Data
5	Vsync	Vertical synchronous signal	25	G1	Green Data
6	DE	Data Enable Signal	26	G0	Green Data (LSB)
7	V_{SS}	GND	27	V_{SS}	GND
8	CLK	Dot Clock	28	R5	Red Data (MSB)
9	V_{SS}	GND	29	R4	Red Data
10	Hsync	Horizontal synchronous signal	30	R3	Red Data
11	V_{SS}	GND	31	V_{SS}	GND
12	B5	Blue Data (MSB)	32	R2	Red Data
13	B4	Blue Data	33	R1	Red Data
14	B3	Blue Data	34	R0	Red Data (LSB)
15	V_{SS}	GND	35	NC	No Connection
16	B2	Blue Data	36	V_{SS}	GND
17	B1	Blue Data	37	NC	No Connection
18	B0	Blue Data (LSB)	38	NC	
19	V_{SS}	GND	39	NC	
20	G5	Green Data (MSB)	40	NC	

Note 1: Please refer to 9.5 SCAN DIRECTION for the setting methods of UD, LR function.

Note 2: Synchronous or DE mode would be automatically selected when signal input.

The backlight interface connector is BHR-03VS-1 made by JAE, and pin assignment of backlight is as below:

Pin No.	Signal	Level	Function
1	V_{LED}+	-	Power Supply for LED
2	NC	-	No connection
3	V_{LED}-	-	GND

LVDS_Rev. A and Rev. B are identical

9.1 INTERFACE PIN CONNECTIONS

The display interface connector (CN1) is FI-SEB20P-HF13E made by JAE and pin assignment is as below:

Pin No.	Signal	Signal	Pin No.	Signal	Signal
1	V_{DD}	Power Supply for Logic	11	IN2-	B2~B5, DE
2	V_{DD}		12	IN2+	
3	UD	Vertical Display mode Control (Note 2)	13	V_{SS}	GND
4	LR	Horizontal Display mode Control (Note 2)	14	CLK IN-	Pixel Clock
5	IN0-	R0~R5, G0	15	CLK IN+	
6	IN0+		16	V_{SS}	GND
7	V_{SS}	GND	17	NC	No Connection
8	IN1-	G1~G5, B0~B1	18	NC	No Connection
9	IN1+		19	NC	No Connection
10	V_{SS}	GND	20	NC	No Connection

Note 1: IN n- and IN n+ (n=0, 1, 2), CLK IN- and CLK IN+ should be wired by twist-pairs or side-by-side FPC patterns, respectively.

Note 2: Please refer to 9.8 SCAN DIRECTION for the setting methods of UD, LR function.

The backlight interface connector (CN2) is BHR-03VS-1 made by JST, and pin assignment is as below:

Pin No.	Signal	Level	Function
1	V_{LED}+	-	Power Supply for LED
2	NC	-	No Connection
3	V_{LED}-	-	GND

Thank you